CLAIMS

What is claimed is:

1. An apparatus for reducing worst-case power consumption, comprising:

a first signal having signal transitions;

a circuit path for transmitting a second signal through buffered circuit sections;

logic circuitry coupled to the circuit path and to the first signal, wherein the logic circuitry uses the first signal to reduce a sum of signal transitions of the second signal as the second signal propagates from one buffered section of the circuit path to another buffered section of the circuit path in order to reduce worse-case power consumption.

2. The apparatus of claim 1, wherein the logic circuitry comprises exclusive-OR (XOR) circuitry.

3. The apparatus of claim 1, wherein the first signal comprises a signal with regular periodic transitions.

4. The apparatus of claim 1, wherein the logic circuitry comprises at least two exclusive-OR (XOR) gates located in the circuit path.

5. The apparatus of claim 1, wherein the buffered circuit sections include a first buffered circuit section, a second buffered circuit section, and a third buffered circuit section; and wherein the logic circuitry causes the second signal to have altered signal transitions in the second buffered circuit section in order to reduce worst-case power consumption.

6. The apparatus of claim 5, wherein the second signal has the same signal transitions in the first and second buffered circuit sections.

7. The apparatus of claim 1, further comprising registers for buffering the buffered circuit sections.

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8. An apparatus comprising:

a first exclusive-OR (XOR) circuit having a first input coupled to the circuit to provide the first data, a second input to receive a periodic signal; and an output to provide the first data in a second format; and

a second XOR circuit having a first input coupled to the output of the first XOR circuit, a second input coupled to receive the periodic signal, and an output to provide the first data in the first format.

9. The apparatus of claim 8, further comprising memory for storing the first data in the second format.

10. The apparatus of claim 9, wherein the periodic signal comprises an address signal for addressing the memory.

11. The apparatus of claim 10, wherein the address signal is generated by a burst counter.

12. The apparatus of claim 8, further comprising:

a plurality of memories for storing the first data in the second format;

a burst counter for generating addresses for storing the first data in the first format, wherein the periodic signal is derived from the addresses,

wherein the first XOR circuit, the second XOR circuit, and the burst counter reside on a buffer chip.

13. The apparatus of claim 8, wherein the second format is different from the first format.

14. The apparatus of claim 8, further comprising:

a first buffer coupled to the output of the first XOR circuit and to the first input of the second XOR circuit;

a second buffer coupled to the output of the second XOR circuit.

15. An apparatus comprising:

a first circuit having a plurality of terminals;

a first plurality of exclusive-OR (XOR) circuits each having a first input coupled to one of the plurality of terminals, a second input coupled to receive a first periodic signal, and an output; and

a second circuit having a first plurality of terminals each coupled to an output of one of the first plurality of XOR circuits, and a second plurality of terminals, wherein a number of the first plurality of terminals is different than a number of second plurality of terminals.

16. The apparatus of claim 15, wherein the second circuit comprises a serializer.

17. The apparatus of claim 16, wherein the serializer comprises a shift register.

18. The apparatus of claim 15, further comprising:

a second plurality of XOR circuits each having a first input coupled to one of the first plurality of terminals of the second circuit, a second input coupled to receive the first periodic signal, and an output coupled to one of the plurality of terminals of the first circuit.

19. The apparatus of claim 18, wherein the second circuit comprises a deserializer.

20. The apparatus of claim 19, wherein the deserializer comprises a shift register.

21. The apparatus of claim 18, further comprising:

a second plurality of XOR circuits each having a first input coupled to one of the second plurality of terminals of the second circuit, a second input coupled to a second periodic signal, and an output.

22. The apparatus of claim 21, wherein the first inputs of the first plurality of XOR gates are each coupled to the first circuit to receive first data in the first format at a first data rate of the first periodic signal, and the outputs of the first plurality of XOR gates are structured to provide the first data in a second format to the second circuit, and wherein the first inputs of the second plurality of XOR gates are each coupled to the second circuit to receive the first data in the second format at a second data rate of the second periodic signal, and the outputs of the second plurality of XOR gates are structured to output the first data in a third format.

23. The apparatus of claim 22, wherein the first data rate of the first periodic

signal is an integer multiple of the second data rate of the second periodic signal.

24. The apparatus of claim 22, wherein the first circuit comprises memory for storing the first data, and wherein the first periodic signal comprises a first address signal for addressing the memory, and the second periodic signal comprises a second address signal for addressing the memory.

25. A system comprising:

a first device comprising:

a first circuit;

a first plurality of exclusive-OR (XOR) circuits having first inputs coupled to receive first data from the first circuit, second inputs each coupled to receive a bit of a first predetermined number, and outputs; and

a second device comprising:

a second plurality of exclusive-OR (XOR) circuits having first inputs coupled to the outputs of the first plurality of XOR circuits, and second inputs coupled to receive one bit of the first predetermined number.

26. The system of claim 25, wherein the first device further comprises a second circuit for storing the first predetermined number.

27. The system of claim 26, wherein the second circuit comprises a pseudo-random number generator.

28. The system of claim 26, wherein the second circuit comprises a memory circuit.

29. The system of claim 25, wherein the first predetermined number

comprises only one bit.

30. The system of claim 25, wherein:

the second device further comprises a third plurality of XOR circuits having first inputs to receive second data, second inputs each coupled to receive a bit of a second predetermined number, and outputs; and

the first device further comprises a fourth plurality of XOR circuits having first inputs coupled to the outputs of the third plurality of XOR circuits, second inputs each coupled to receive a bit of the second predetermined number, and outputs coupled to the first circuit.

31. The system of claim 30, wherein the first predetermined number and the second predetermined number are the same number.

32. The system of claim 30, wherein the second predetermined number is only one bit.

33. An apparatus comprising:

a first circuit;

a first plurality of exclusive-OR (XOR) circuits having first inputs coupled to receive first data from the first circuit, second inputs each coupled to receive a bit of a predetermined number; and

a second circuit providing the first predetermined number to the first plurality of XOR circuits.

34. The apparatus of claim 33, further comprising:

a second plurality of XOR circuits having first inputs coupled to outputs of

the first plurality of XOR circuits, second inputs coupled to the predetermined number, and outputs coupled to the first circuit.

35. The apparatus of claim 33, wherein the predetermined number is only bit.

36. The apparatus of claim 33, wherein the second circuit comprises a pseudo-random number generator.

37. The apparatus of claim 33, wherein the first circuit comprises a memory circuit, and the second circuit comprises a memory location within the first circuit.

38. A method of reducing power drawn by two circuits comprising;

determining the worst-case data pattern that results in drawing maximum amounts of power from the two circuits; and

passing the worst-case data pattern from one of the circuits through at least one exclusive-OR (XOR) gate to reduce power drawn by that circuit.

39. A method of accessing a memory device comprising:

writing data to the memory device via a first exclusive-OR (XOR) gate clocked by a periodic signal.

40. The method of claim 39, further comprising the step of

reading data from the memory device via a second XOR gate clocked by the periodic signal.

41. A method of accessing a memory device comprising:

providing first data to a bus interface of the memory device in a first format and at a first data rate;

reformatting the first data to a second format in response to an address

signal, the second format having a second data rate different than the first data rate;

and storing the reformatted data in the memory device in the second format.

42. The method of claim 41, wherein the step of storing the reformatted data comprises storing uncomplemented first data at even addresses, and storing complemented first data at odd addresses of the memory device.

43. The method of claim 41, further comprising:

reformatting the stored data into the first format; and

outputting the data in first format from the bus interface.

44. A memory device for interfacing with a data bus and an address bus, the memory device comprising:

a reformatting circuit receiving data in a first format at a first data rate from the data bus, and reformatting the data to a second format in response to an address signal on the address bus that alternates at the first data rate, the reformatted data having a second data rate that is different than the first data rate; and

a memory circuit coupled to the reformatting circuit and storing the reformatted data.

45. The memory device of claim 44, wherein the reformatting circuit comprises an exclusive-OR (XOR) gate having a first input coupled to the data bus, a second input coupled to the address signal, and an output coupled to the

memory circuit.

46. The memory circuit of claim 44, wherein the reformatting circuit reformats the reformatted data in response to the address signal to regenerate the data having the first format and the first data rate.

47. The memory circuit of claim 46, wherein the reformatting circuit comprises an exclusive-OR (XOR) gate having a first input coupled to the memory circuit, a second input coupled to the address signal, and an output coupled to the data bus.